

Table of Contents

	Topic	Page No.
1	Introduction	1
2	Background	3
	2.1 Partitioning	3
	2.2 Multi-Personality Partitioning	4
	2.3 Content-Aware Partitioning	5
3	Benchmarks for Multi-Personality Partitioning	7
	3.1 Potential Benchmark Sources	7
	3.2 Benchmark Requirements	9
	3.3 Benchmark Evaluation	10
	3.3.1 HDL Benchmarks	10
	3.3.2 Non-HDL Benchmarks	15
	3.4 Selected Benchmarks	17
	3.5 HDL Benchmark Processing	19
	3.5.1 HDL Synthesis	20
	3.5.2 HDL Parsing	20
	3.5.3 Graph Formation	21
	3.5.3 Resource Weight Assignment	22

3.6	Non-HDL Benchmark Processing	22
3.7	Benchmark Use	23
4	Benchmarks for Content-Aware Partitioning	25
4.1	Benchmark Requirements	25
4.2	Benchmark Evaluation	25
4.3	Benchmark Processing	27
5	Conclusion	29
6	References	30
7	Appendix 1: LUT, DSP and BRAM resource estimates for GTECH library components	35
8	Appendix 2: Synthesizing and running workloads with Amber, an ARM-based core	42
8.1	Synthesis	42
8.2	Post-Synthesis Verification	43
8.3	Compiling In-Package Workloads	43
8.4	Custom Workloads for Amber	46
8.4.1	Workload Sources	46
8.4.2	Adapting Custom Workloads for Amber – I	46
8.4.3	Workload Conversion from C to Assembly	48
8.4.4	Adapting Custom Workloads for Amber – II	48
8.4.5	Compiling Custom Workloads	49

8.5	Running Workloads on Amber	49
8.6	Setup Summary	49
8.7	RAM Generation	50
8.8	Environment Details	50
8.9	References	50

List of Tables

Table	Page No.
Table 1: ERCBench circuits and their application areas	17
Table 2: DIMACS graph categories	19
Table 3: Selection of benchmarks	20
Table 4: Characterization of selected benchmarks	21
Table 5: LUT Estimate Calculations for GTECH components	35
Table 6: LUT, DSP and BRAM Estimates for GTECH components	38

List of Figures

Figure	Page No.
Figure 1: Typical CAD flow that includes a partitioning step	8
Figure 2: Illustration of cut size	8
Figure 3: (a) Catalogue output of the parser; (b) Intermediate netlist representation sample	26

List of Abbreviations

Symbol	Explanation
ASIC	Application Specific Integrated Circuit
BLIF	Berkeley Logic Interchange Format
BRAM	Block Ram
CAD	Computer Aided Design
CLB	Configurable Logic Blocks
DIMACS	Discrete Mathematics and Theoretical Computer Science
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
IMC	Internet Measurement Conference
IP	Intellectual Property
ISCAS	International Symposium on Circuits and Systems
ITC	International Test Conference
IWLS	International Workshop on Logic and Synthesis
LUT	Look Up Table

Symbol	Explanation
MAC	Multiply Accumulate
MCNC	Microelectronics Center of North Carolina
PREP	Programmable Electronics Performance Corporation
RAM	Random Access Memory
RTL	Register-Transfer Level
VHDL	Very High Speed Integrated Circuits Hardware Description Language