WiscF12 16-Bit Processor with 5-Stage Pipeline

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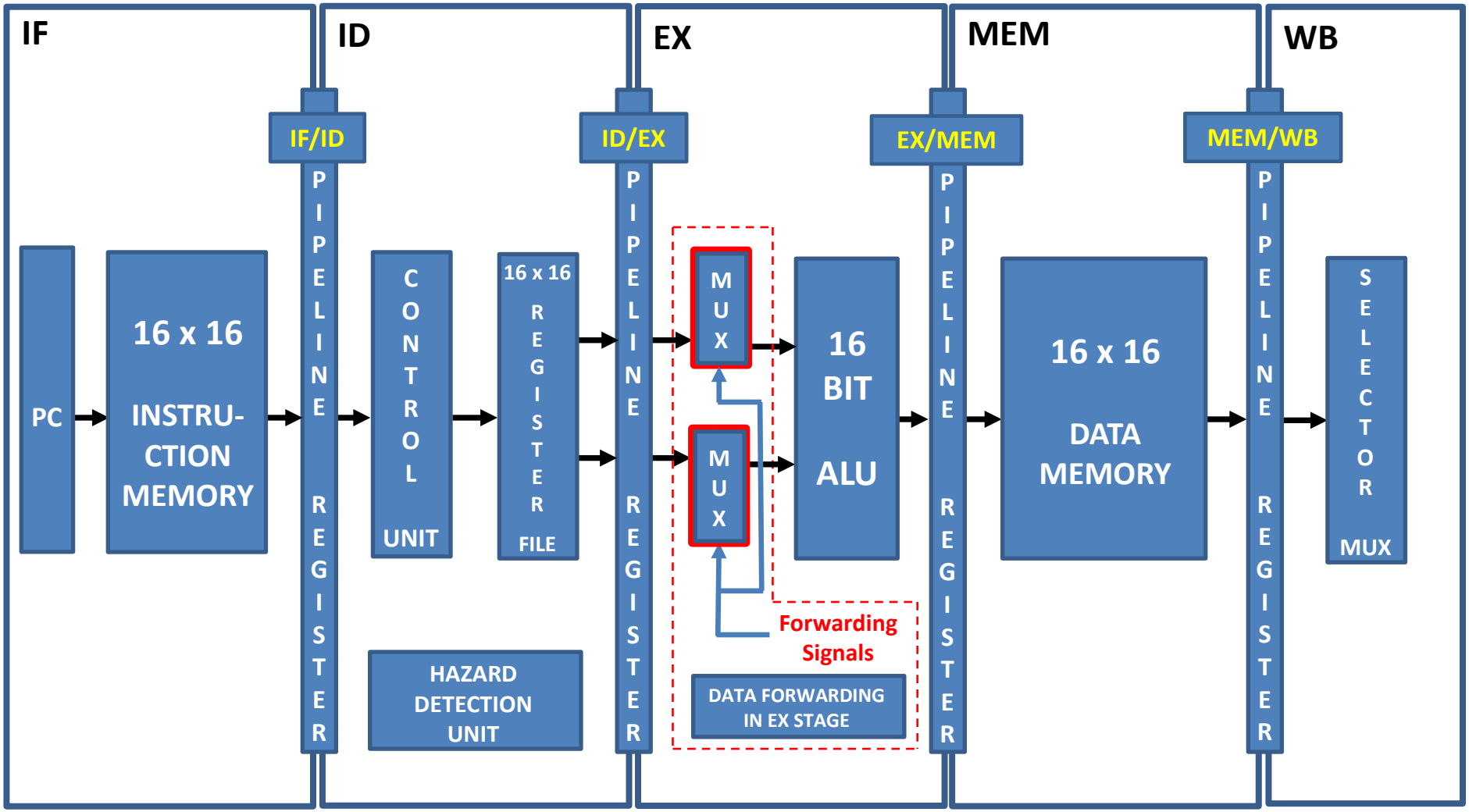
Processor Overview

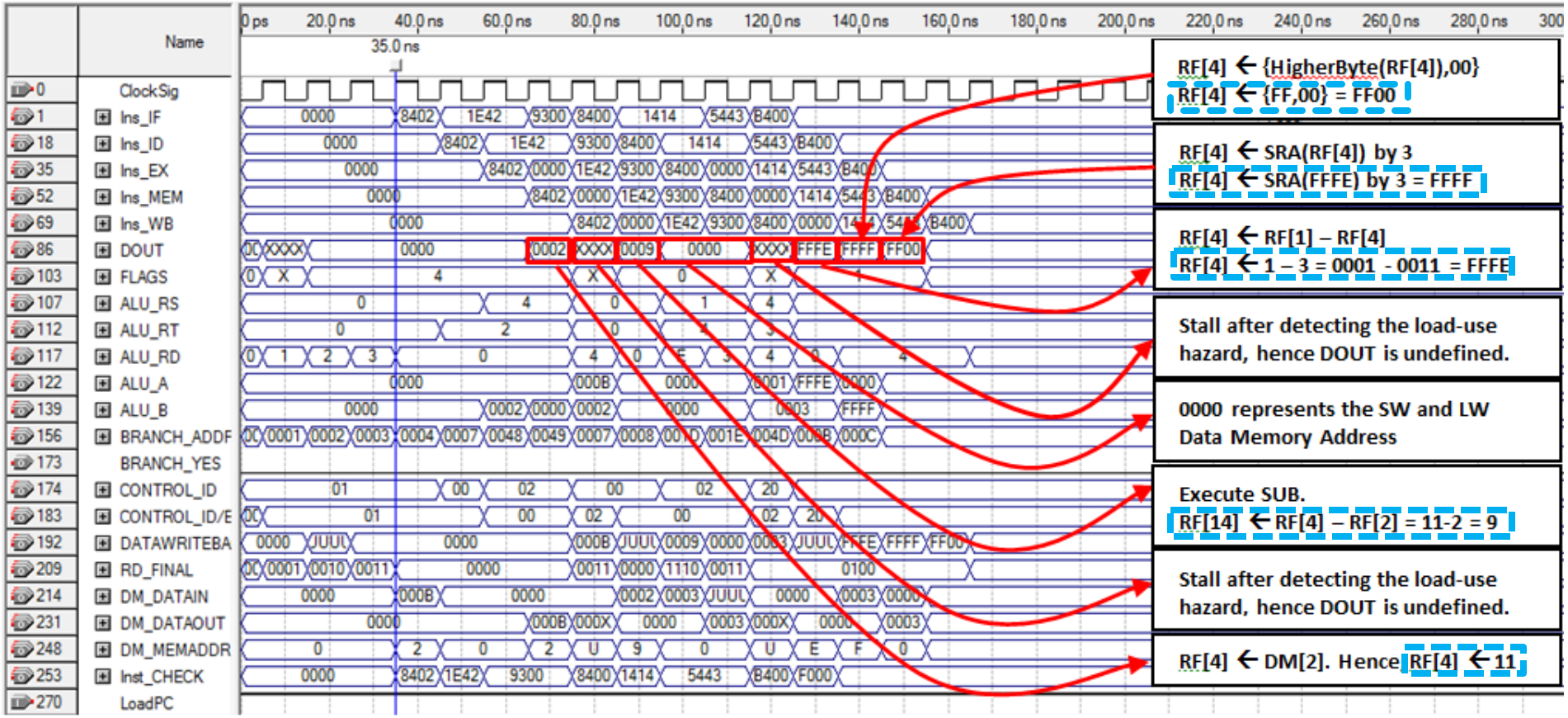


Features Implemented

- Data Hazard Detection; Forwarding
  - RAW (True Data Dependence) leads to Data Hazards
  - *Integral problem associated with pipelining*
  - Solution lies in Forwarding; processor does just that
  - Hazard Detection in ID stage; forwarding implemented in the EX stage
- Stalling
  - Dependencies involving LW in particular *need a Stall even after forwarding*, so stalling was implemented as well
- Flushing
  - *Control Hazard*: the pipeline stages before the stage of CALL/RET/B instructions are flushed
- Verification and Testing
  - Tried out all the *Test Bench programs* to ensure design correctness

TestBench – Program 2 - *Pipelined*
(Load-Use Hazard)

RF[1]=1, RF[2]=2, RF[3] = 3, DM[2]=11



LW $4, 2 SUB $14, $4, $2 SW $3, 0 LW $4, 0 SUB $4, $1, $4 SRA $4, $4, 3 LLB $4, 0 HALT

Flow Summary

Flow Status	Successful - Tue Dec 11 23:48:51 2012
Quartus II Version	9.0 Build 235 06/17/2009 SP 2 SJ Web Edition
Revision Name	552
Top-level Entity Name	Entire
Family	Stratix
Met timing requirements	Yes
Logic utilization	11 %
Combinational ALUTs	850 / 12,480 (7 %)
Dedicated logic registers	868 / 12,480 (7 %)
Total registers	868
Total pins	247 / 343 (72 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP1S80F1508C5
Timing Models	Final

Timing Analyzer Summary

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock
1	Worst-case tsu	N/A	None	4.831 ns	LoadPC	PC:inst91|pcounter:inst|lpm_ff:lpm_ff_component|dffs[3]	--	ClockS
2	Worst-case tco	N/A	None	12.692 ns	Pipeline16:inst57|lpm_ff:lpm_ff_component|dffs[15]	Ins_IF[9]	ClockSig	--
3	Worst-case tpd	N/A	None	9.074 ns	LoadPC	PCId	--	--
4	Worst-case th	N/A	None	0.226 ns	DM_Load[0]	Pipeline16:inst42|lpm_ff:lpm_ff_component|dffs[0]	--	ClockS
5	Clock Setup: 'ClockSig'	N/A	None	137.04 MHz (period = 7.297 ns)	Pipeline1:inst70|lpm_ff:lpm_ff_component|dffs[0]	ALU:inst77|flagff:inst17|lpm_ff:lpm_ff_component|dffs[0]	ClockSig	ClockS
6	Total number of failed paths							

Thank You!